FORM PTO-1390 (REV. 11-2000) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER	
0152-0577P	
U.S. APPLICATION NO. (If known, see 37 CFR 1.5)	
09/914077 NEW	

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/JP00/01029	February 23, 2000	February 24, 1999

TITLE OF INVENTION
IC DEVCIE AND ITS PRODUCTION METHOD, AND INFORMATION CARRIER MOUNTED WITH IC DEVICE AND ITS PRODUCTION METHOD

APPLICANT(S) FOR DO/EO/US
KAWAMURA, Satoshi; SHIMIZU, Shin

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39 (1).
4. ☐ The US has been elected by the expiration of 19 months from the priority date (Article 31).
5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☒ has been transmitted by the International Bureau. WO 00/51181
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. ☒ is transmitted herewith.
   b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4)
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3)).
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.
8. ☐ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☐ An English language translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11. to 20. below concern document(s) or information included:

11. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.-1449 and International Search Report (PCT/ISA/210) w/. 6 cited documents.
12. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☒ A FIRST preliminary amendment.
14. ☐ A SECOND or SUBSEQUENT preliminary amendment.
15. ☐ A substitute specification.
16. ☐ A change of power of attorney and/or address letter.
17. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821-1.825.
18. ☐ A second copy of the published international application under 35 U.S.C. 154(d)(4).
19. ☐ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
20. ☒ Other items or information:
    Ten (10) sheets of formal drawings

U.S. APPLICATION NO (If known, see 37 CFR 1.5)	INTERNATIONAL APPLICATION NO	ATTORNEY'S DOCKET NUMBER
09/914077	PCT/JP00/01029	0152-0577P

21. ☒ The following fees are submitted:

	CALCULATIONS	PTO USE ONLY
BASIC NATIONAL FEE (37 CFR 1.492(a)(1)-(5):		
Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO **$1,000.00**		
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO **$860.00**		
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO **$710.00**		
International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4) **$690.00**		
International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) **$100.00**		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$ 860.00	
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$ 0.00	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total Claims	27 - 20 =	7	X **$18.00**	$ 126.00	
Independent Claims	12 - 3 =	9	X **$80.00**	$ 720.00	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)		NONE	+ **$270.00**	$ 0.00	
			TOTAL OF ABOVE CALCULATIONS =	$ 1,720.00	
☐ Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by 1/2.				$ 0.00	
			SUBTOTAL =	$ 1,720.00	
Processing fee of **$130.00** for furnishing the English translation later than ☐20 ☐30 months from the earliest claimed priority date (37 CFR 1.492(f)). +				$ 0.00	
			TOTAL NATIONAL FEE =	$ 1,720.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property +				$ 40.00	
			TOTAL FEES ENCLOSED =	$ 1,746.00	
				Amount to be: refunded	$
				charged	$

a. ☒ A check in the amount of $ **1,746.00** to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account. No. _____ in the amount of $_____ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 02-2448.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

Send all correspondence to:
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Date: August 23, 2001

By _____
Joseph A. Kolasch, #22,463

/REM

PATENT
0152-0577P

IN THE U.S. PATENT AND TRADEMARK OFFICE

Applicant:	KAWAMURA, Satoshi et al.	Conf.:	
Int'l. Appl. No.:	PCT/JP00/01029		
Appl. No.:	NEW	Group:	
Filed:	August 23, 2001	Examiner:	
For:	IC DEVCIE AND ITS PRODUCTION METHOD, AND INFORMATION CARRIER MOUNTED WITH IC DEVICE AND ITS PRODUCTION METHOD		

PRELIMINARY AMENDMENT

BOX PATENT APPLICATION
Assistant Commissioner for Patents
Washington, DC 20231

August 23, 2001

Sir:

The following Preliminary Amendments and Remarks are respectfully submitted in connection with the above-identified application.

AMENDMENTS

After line 1, insert --This application is the national phase under 35 U.S.C. § 371 of PCT International Application No. PCT/JP00/01029 which has an International filing date of February 23, 2000, which designated the United States of America and was not published in English.--

IN THE CLAIMS:

Please amend the claims as follows:

18. (Amended) An information carrier set forth in claim 16, characterized in that said recess is formed circularly in a plane shape.

REMARKS

The specification has been amended to provide a cross-reference to the previously filed International Application. The claims have also been amended to delete multiple dependencies.

Entry of the above amendments is earnestly solicited. An early and favorable first action on the merits is earnestly solicited.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

BIRCH, STEWART, KOLASCH & BIRCH, LLP

By _____
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JAK/rem
0152-0577P

Attachment: VERSION WITH MARKINGS TO SHOW CHANGES MADE

VERSION WITH MARKINGS TO SHOW CHANGES MADE

The specification has been amended to provide cross-referencing to the International Application.

IN THE CLAIMS:

The claims have been amended as follows:

18. (Amended) An information carrier set forth in claim 16 [or claim 17], characterized in that said recess is formed circularly in a plane shape.

DESCRIPTION

IC DEVICE AND ITS PRODUCTION METHOD, AND INFORMATION CARRIER MOUNTED WITH IC DEVICE AND ITS PRODUCTION METHOD

TECHNICAL FIELD

The present invention relates to AN IC element formed integrally with a coil on a chip, a method of manufacturing the IC element, an information carrier incorporating the IC element and a method of manufacturing the information carrier.

BACKGROUND ART

Heretofore, such a contactless type information carrier has been known which includes an IC element mounted internally of a substrate having a predetermined shape and an antenna coil electrically connected to the terminals of the IC element for effectuating in a noncontacting or contactless manner reception of electric power from a reader/writer and a signal transmission/reception with the reader/writer through the medium of the electromagnetic wave. As the information carriers of this species, there may be mentioned those referred to as the card-like information carriers, the coin-like information carriers, the button-like information carriers and the like named after the external appearance.

As the information carriers of the types

mentioned above, the information carrier having an antenna coil patterned on a substrate or the information carrier having an antenna coil composed of a coil carried on a substrate has heretofore been employed. However, in recent years, there has been proposed an information carrier in which the IC element formed integrally with the antenna coil is mounted on the substrate and which features the capability of being manufactured inexpensively without need for the protection processing of the interconnection points between the antenna coil and the IC element and the moisture-proof treatment and additionally the excellent durability owing to insusceptibility to breakage of coil conductor regardless of stresses induced upon bending, torsion or the like of the substrate.

As a method of forming the antenna coil on the information carrier, a sputtering method is adopted. Thus, the electric conductor of the antenna coil formed integrally with the IC element is implemented in the form of an aluminum-sputtered film.

In this conjunction, it is however noted that when the antenna coil is formed integrally on the IC element, not only the winding diameter and the conductor width of the coil become smaller when compared with the case where the antenna coil composed of the winding is carried on the substrate, but also the number of turns of the coil is naturally limited, making it difficult to increase the range or distance

for communication with the reader/writer or rendering it even impossible to ensure the communication range.

The present invention has been made with a view to disposing of the deficiencies of the hitherto known techniques such as mentioned above and hence it is contemplated with the present invention as a technical object to provide an information carrier incorporating an IC element formed integrally with an antenna coil and capable of ensuring an extended communication range or distance and a method of manufacturing the information carrier as well as a structure of the IC element formed integrally with the antenna coil and advantageously suited for employment in the information carrier of this sort and a method of manufacturing the IC element.

DISCLOSURE OF THE INVENTION

For accomplishing the object mentioned above, the present invention provides an IC element formed integrally with a coil, wherein a conductor constituting the above-mentioned coil is implemented in a multilayer structure including a metal-sputtered layer or alternatively a metal-evaporated layer and a metal-plated layer.

Since the metal-plated layer has an electric resistance value smaller than the metal-sputtered layer or alternatively the metal-evaporated layer, loss of the electromagnetic energy can be diminished by

implementing the electric conductor of the coil in a multilayer structure composed of the metal-sputtered layer or alternatively the metal-evaporated layer and the metal-plated layer when compared with the coil conductor constituted solely by the metal-sputtered layer or alternatively the metal-evaporated layer, whereby the distance or range for communication with the reader/writer can be increased.

<IC element manufacturing method>

For achieving the object mentioned previously, there is provided according to a first aspect of the present invention an IC element manufacturing method which includes a step of forming uniformly a metal-sputtered layer or alternatively a metal-evaporated layer on a surface passivation film of a finished wafer manufactured through a predetermined process, a step of forming uniformly a photoresist layer on said metal-sputtered layer or alternatively on said metal-evaporated layer, a step of exposing said photoresist layer to light illumination in a predetermined pattern inclusive of a coil for thereby exposing said metal-sputtered layer or alternatively said metal-evaporated layer in said predetermined pattern after development, a step of laminating a metal-plated layer on exposed portions of said metal-sputtered layer or alternatively said metal-evaporated layer through an electroless plating method or alternatively an electroplating method or alternatively

through a precision electroforming method, a step of eliminating the photoresist layer deposited on said finished wafer, a step of forming a predetermined conductor pattern corresponding to said predetermined pattern by etching said metal-sputtered layer or alternatively said metal-evaporated layer exposed through said metal-plated layer, and a step of obtaining a concerned IC element formed integrally with the coil by scribing said finished wafer.

Further, according to a second aspect of the present invention, there is provided a method which includes a step of forming uniformly a photoresist layer on a surface passivation film of a finished wafer manufactured through a predetermined process, a step of exposing in said photoresist layer to light illumination in a predetermined pattern inclusive of a coil for thereby exposing said surface passivation film in said predetermined pattern after develop-ment, a step of mounting the finished wafer undergone the development processing on a sputtering apparatus or a vacuum evaporation apparatus for forming a metal-sputtered layer or alternatively a metal-evaporated layer on exposed portion of said surface passivation film, a step of eliminating the photoresist layer deposited on said finished wafer, a step of laminating a metal-plated layer on said metal-sputtered layer or alternatively said metal-evaporated layer through an electroless plating method or alternatively through an

electroplating method, and a step of obtaining a concerned IC element formed integrally with a coil by scribing said finished wafer.

As is apparent from the above, by forming the required electric conductive pattern inclusive of the coil on the finished wafer to thereby obtain the concerned IC element by scribing the finished wafer, the IC element formed integrally with the coil can be manufactured with high efficiency when compared with the case where each of the individual IC elements are formed with a coil, whereby the manufacturing cost can be reduced. Furthermore, it is possible to implement the coils of a uniform thickness with high precision for all the IC elements formed on the wafer, whereby variance or dispersion of the communication characteristics can be suppressed.

Furthermore, it is noted that when the coil is formed for each of the individual IC elements by using the sputtering method or alternatively the vacuum evaporation method and the plating method, there arises a problem concerning the insulation quality of the IC element due to deposition of unnecessary conductors on an outer peripheral portion of the IC element. Of course, when the required electric conductive pattern inclusive of the coil is formed on the finished wafer, the unnecessary conductors may be deposited on the outer peripheral portion of the finished wafer upon sputtering or the like process. However, the outer

peripheral portion mentioned just above is intrinsically to be disposed of as the unnecessary portion. Accordingly, there will arise no problem in respect to the insulation quality of the individual IC elements.

<IC>

For achieving the object mentioned previously, the present invention provides an information carrier including a substrate having mounted thereon an IC element formed integrally with an antenna coil, wherein said IC element is disposed at a center portion of said substrate in a planar direction perpendicular to a plane of said substrate.

By disposing the IC element on the substrate at the center portion as viewed in the planar direction of the substrate as mentioned above, the center of the coil formed integrally with the IC element and that of the antenna coil for the reader/writer can be easily aligned to each other. Thus, the coefficient of the electromagnetic coupling between both coils can be increased, whereby the electric power supply to the information carrier from the reader/writer as well as the signal transmission/reception between the reader/writer and the information carrier can be carried out with enhanced reliability. In particular, when the substrate which constitutes the information carrier is shaped in a square shape, a regular-polygonal shape or the like which exhibits no or less directivity relative to the reader/writer, the center

of the coil formed integrally on the IC element can be aligned more easily with that of the antenna coil provided for the reader/writer, which allows the information carrier to be handled more facilitatively.

For achieving the object mentioned previously, an IC manufacturing method provided according to a first aspect of the present invention includes a step of bonding together a first strip material having regularly formed therein a number of through-holes in which IC elements can be inserted, respectively, and a second strip material formed with no through-hole, a step of placing and fixing the IC elements each formed integrally with a coil in said through-holes, respectively, a step of bonding together said first strip material and a third strip material having no through-hole, and a step of punching said first to third integrally bonded strip materials to thereby obtain the concerned information carriers each incorporating said IC element.

Further, an IC manufacturing method provided according to a second aspect of the present invention includes a step of placing and fixing coils formed discretely independent of IC elements, respectively, in a number of ring-like recesses formed in a first strip material concentrically around through-holes, which are formed regularly in said first strip material and in which said IC elements can be inserted, respectively, a step of bonding a second strip material having no

through-hole onto one surface of said first strip material, a step of placing fixedly said IC elements each formed integrally with a coil in said through-holes, respectively, a step of bonding together said first strip material and a third strip material having no through-hole, and a step of punching said first to third strip materials bonded integrally, to thereby obtain desired information carriers each including the IC element and the coil formed discretely independent of said IC element.

As is apparent from the above, the strip lamination in which the required IC elements (or alternatively the IC elements and the coils) are embedded is manufactured, whereon the concerned or desired information carriers are formed by punching the strip lamination. Thus, the identical information carriers can be manufactured with high efficiency, whereby the cost involved in manufacturing the desired information carriers can be reduced.

Incidentally, in the manufacturing methods according to the first and second aspects described above, the substrate of the information carrier is formed of three members (i.e., the first to third strip members), it is equally possible to implement the substrate for the information carrier with two members by forming the recesses for accommodating the IC elements, respectively, in the first strip material instead of adopting the structure in which the through-

holes for accommodating the IC elements, respectively, are formed in the first strip material.

Furthermore, in the manufacturing methods according to the first and second aspects described above, the IC elements (or the IC elements and the coils) are completely embedded internally of the strip materials. However, it is also possible to make the IC elements (or the IC elements and the coils) be exposed exteriorly from one surface of the strip material by sealing off the through-holes or the recesses formed in the strip material with a resin after having placed the IC elements (or the IC elements and the coils) in the through-holes or the recesses, respectively.

Besides, when the IC elements (or the IC elements and the coils) is to be exposed externally of the one surface of the strip material, the substrate of the information carrier can be formed by a single member by forming the recesses for accommodating the respective IC elements (or the IC elements and the coils) in the strip material.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1A, 1B and 1C are plan views showing IC elements according to exemplary embodiments, respectively.

Figures 2A and 2B are sectional views showing major portions of IC elements according to exemplary embodiments, respectively.

Figure 3 is a plan view showing a finished wafer.

Figures 4A, 4B, 4C, 4D, 4E and 4F are views for illustrating stepwise a first example of an IC element manufacturing method according to the present invention.

Figures 5A, 5B, 5C, 5D and 5E are views for illustrating stepwise a second example of the IC element manufacturing method according to the present invention.

Figure 6 is a plan view showing a finished wafer having formed thereon a required electric conductive pattern inclusive of an antenna coil.

Figure 7 is a partially broken plan view of an information carrier according to a first exemplary embodiment.

Figure 8 is a developed perspective view showing the information carrier according to the first exemplary embodiment.

Figure 9 is a sectional view of the information carrier according to the first exemplary embodiment.

Figure 10 is a view illustrating the information carrier according to the first exemplary embodiment in the state being used.

Figure 11 is a sectional view of an information carrier according to a second exemplary embodiment.

Figure 12 is a sectional view of an information carrier according to a third exemplary embodiment.

Figure 13 is a sectional view of an information carrier according to a fourth exemplary embodiment.

Figure 14 is a sectional view of an information carrier according to a fifth exemplary embodiment.

Figure 15 is a sectional view of an information carrier according to a sixth exemplary embodiment.

Figure 16 is a sectional view of an information carrier according to a seventh exemplary embodiment.

Figure 17 is a sectional view of an information carrier according to an eighth exemplary embodiment.

Fig. 18 is a fragmental perspective view showing a first example of a strip material.

Fig. 19 is a fragmental perspective view showing a second example of the strip material.

Fig. 20 is a fragmental perspective view showing a third example of the strip material.

Fig. 21 is a fragmental perspective view showing a fourth example of the strip material.

Fig. 22 is a fragmental perspective view showing a fifth example of the strip material.

BEST MODE FOR CARRYING OUT THE INVENTION

<IC element>

In the following, description will be made of IC elements according to exemplary embodiments of the present invention by reference to Figs. 1A, 1B and 1C together with Figs. 2A and 2B, wherein Figs. 1A, 1B and 1C are plan views showing the IC elements according to the exemplary embodiments, respectively, of the invention and Figs. 2A and 2B are sectional views showing major portions of the IC elements according to the exemplary embodiments, respectively, of the invention.

As is shown in Figs. 1A, 1B and 1C and Figs. 2A and 2B, in each of the IC elements according to the instant exemplary embodiments, an antenna coil 3 of a rectangular spiral pattern is formed integrally on a surface of the IC element 1 in which input/output terminals 1a thereof are formed through the medium of an electrically insulative surface passivation film 2 such as a silicon oxide film, a resin film or the like.

In the case of the IC element 1 shown in Fig. 1A, the antenna coil 3 is formed only in an outer peripheral portion exclusive of a circuit forming portion 4. By virtue of this structure, appearance of stray capacitance between the circuit formed in the IC element 1 and the antenna coil 3 can be prevented, whereby the efficiency of electric power reception from a reader/writer as well as the efficiency of signal

transmission/reception with the reader/writer can be enhanced.

In the case of the IC element 1 shown in Fig. 1B, the antenna coil 3 is so formed as to extend over the circuit forming portion 4. With this structure, the number of turns of the antenna coil can be increased, whereby the efficiency of power reception from the reader/writer as well as the efficiency of signal transmission/reception with the reader/writer can be much enhanced.

Incidentally, in the case of the exemplary embodiment shown in Fig. 1B, the antenna coil is overlaid partially on the circuit forming portion 4. However, it is equally possible to form the antenna coil over the whole circuit forming portion 4 with a view to implementing the IC element in a miniature size at low cost.

In the IC element 1 shown in Fig. 1C, corner portions of the antenna coil 3 formed in a rectangular spiral pattern are chamfered obliquely. Owing to this feature, current concentration in the corner portions can be prevented with the resistance value of the antenna coil 3 being thereby decreased, as a result of which the efficiency of power reception from the reader/writer as well as the efficiency of signal transmission/reception with the reader/writer can be much more enhanced. The corner portion may be chamfered arcuately substantially to the same effect.

Furthermore, although it is preferred to chamfer both the inner and outer peripheral edge portions of the individual turns, only the outer peripheral edge portions may be chamfered substantially to the similar effect.

In any cases of the antenna coils 3 described above, the line width of the antenna coil 3 should preferably be greater than 7 μm inclusive, the inter-turn distance should preferably be shorter than 5 μm inclusive and the number of turns should preferably be greater than 20 turns inclusive in order to ensure that sufficient electric power can be fed to the antenna coil while realizing desirable characteristics for the communication with the reader/writer in practical applications.

Interconnection of the input/output terminals 1a of the IC element 1 and the antenna coil 3 are made through-holes 5 opened in the surface passivation film 2. In that case, the diameter or width of the through-hole 5 should preferably be sized smaller than the line width of the antenna coil 3, as can be seen in Figs. 2A and 2B, so that the input/output terminal 1a and the antenna coil 3 can be interconnected without fail even in the case the position at which the antenna coil 3 is formed deviated more or less from that of the antenna coil.

The conductor constituting the antenna coil 3 is implemented in a multilayer structure which includes

a metal-sputtered layer or alternatively a metal-evaporated layer 6 and a metal-plated layer 7, as shown in Figs. 2A and 2B. In the case of the example shown in Fig. 2A, the metal-plated layer 7 is formed only on the top surface of the metal-sputtered layer or alternatively metal-evaporated layer 6. On the other hand, in the case of the example shown in Fig. 2B, the metal-plated layer 7 is so formed as to cover the whole surface of the metal-sputtered layer or alternatively metal-evaporated layer 6. The metal-sputtered layer or alternatively metal-evaporated layer 6 and the metal-plated layer 7 can be formed of a given electrically conductive metal or metals. However, it is preferred to form the metal-sputtered layer or alternatively metal-evaporated layer 6 of aluminum or nickel or copper or chromium because of relatively low cost and high electric conductivity. Further, the antenna coil can be formed in a single layer or in a laminated structure including a combination of plural layers, as can be seen in Figs. 2A and 2B. The metal-plated layer 7 should preferably be formed of copper by resorting to a non-electrolytic plating method or an electroplating method or a precision electroforming method.

<IC element manufacturing method>

Next, description will be made of exemplary embodiments of the IC element manufacturing method according to the present invention by reference to Figs. 3 to Fig. 6, wherein Fig. 3 is a plan view of a

so-called finished wafer which has been completed through predetermined treatment processes, Figs. 4A, 4B, 4C, 4D, 4E and 4F are views for illustrating stepwise a first example of the IC element manufacturing method according to the present invention, Figs. 5A, 5B, 5C, 5D and 5E are views for illustrating stepwise a second example of the IC element manufacturing method according to the present invention, and Fig. 6 is a plan view of a finished wafer having formed thereon a required conductive pattern inclusive of the antenna coil.

As is shown in Fig. 3, a large number of circuits 12 for the IC element are formed with equidistance in an inner portion exclusive of the outermost peripheral portion, wherein the surface passivation film 2 is formed over the surface on which the circuits for the IC element are formed (see Figs. 4 and 5).

In the IC element manufacturing method according to a first exemplary embodiment shown in Figs. 4A, 4B, 4C, 4D, 4E and 4F, the metal-sputtered layer or alternatively metal-evaporated layer 6 is formed uniformly on the surface passivation film 2 deposited on the circuit-formed surface of the finished wafer 11 by using aluminum or an aluminum alloy or alternatively copper or a copper alloy, as is shown in Fig. 4A. Subsequently, a photoresist layer 12 is uniformly formed on the metal-sputtered layer or

alternatively metal-evaporated layer 6 and then the photoresist layer as formed is covered with a mask 13 of a required pattern inclusive of the coils, whereon the photoresist layer 12 is exposed to illumination of light rays 14 of a predetermined wavelength externally of the mask 13, as is shown in Fig. 4B. Thereafter, the photoresist layer 12 undergone the light exposure is subjected to a developing process, whereby the light-exposed portions of the photoresist layer 12 are removed, as a result of which the portions of the metal-sputtered layer or alternatively metal-evaporated layer 6 which correspond to the above-mentioned light exposure pattern is exposed outwardly, as is shown in Fig. 4C. The exposure pattern of the metal-sputtered layer or alternatively metal-evaporated layer 6 includes a ring-shaped electrode portion 15, the antenna coils 3 formed on the portions opposite to the aforementioned circuits 12, respectively, and lead portions 16 for connecting the individual antenna coils 3 and the electrode portion 15, as is shown in Fig. 6. In succession, by making use of the above-mentioned electrode portion 15 as one electrode, electroplating or precision electroforming process is performed on the exposed portions of the metal-sputtered layer or alternatively metal-evaporated layer 6, to thereby laminate the metal-plated layers 7 on the exposed portions of the metal-sputtered layer or alternatively metal-evaporated layer 6, as is shown in Fig. 4D.

Subsequently, the photoresist layer 12 deposited on the surface of the finished wafer 11 is removed through an ashing or the like process to thereby obtain the finished wafer 11 formed with the metal-plated layer 7 including the electrode portion 15, the antenna coils 3 and the lead portions 16 deposited on the uniform metal-sputtered layer or alternatively metal-evaporated layer 6, as shown in Fig. 4E. In succession, the metal-sputtered layer or alternatively metal-evaporated layer 6 exposed through the metal-plated layer 7 is selectively etched to thereby remove the metal-sputtered layer or alternatively metal-evaporated layer 6 exposed externally through the metal-plated layer 7, as is shown in Fig. 4F. Thus, there is obtained the finished wafer 11 on which both the metal-sputtered layer or alternatively metal-evaporated layer 6 and the metal-plated layer 7 are formed in the required conductive pattern shown in Fig. 6. Finally, the finished wafer 11 mentioned just above is scribed to obtain the desired IC elements 1 shown in Fig. 1.

Incidentally, in the exemplary embodiment described above, the electroplating method or precision electroforming method is adopted as the process for forming the metal-plated layer 7. It should however be understood that instead of these methods, an electroless plating method may be resorted to for forming the metal-plated layer 7 mentioned above. In that case, since no electrode is required for forming

the metal-plated layer 7, it is unnecessary to form the electrode portion 15 and the lead portions 16 upon exposure of the photoresist layer 12 to light illumination.

The electroless plating method is also referred to as the chemical plating and destined for deposition of metal ions by immersing a substrate metal in a bath containing a metallic salt solution of plating metal. The electroless plating method features that a metal-plated layer which exhibits high adhesion and having a uniform and adequate thickness can be formed with relatively simple equipment. The metallic salt mentioned above serves as a supply source of metal ions to be deposited. For plating with copper, a solution of copper sulfate, cupric chloride, copper nitrate or the like is used as the plating solution. The metal ions such as copper ions or the like ions are deposited only on the metal-sputtered layer or alternatively metal-evaporated layer 6 serving as the substrate and not deposited on the electrically insulative surface passivation film 2 (or passivation film). The substrate is required to exhibit less ionization tendency for the plating metal ions and exhibit a catalytic action for deposition of the plating metal ions. Such being the circumstances, when the metal-sputtered layer or alternatively metal-evaporated layer 6 formed of aluminum is to be plated with copper, it is preferred to carry out a

pretreatment of forming a nickel film of several μm or less in thickness on the surface of the aluminum layer for substituting nickel for zinc by immersing in a zinc nitrate solution for several seconds.

On the other hand, in the electroplating method and the precision electroforming method, the finished wafer 11 having the metal-sputtered layer or alternatively metal-evaporated layer 6 formed thereon and an electrode made of a plating metal are immersed in a plating bath containing plating metal ions, whereon a voltage is applied across the metal-sputtered layer or alternatively metal-evaporated layer 6 formed on the finished wafer 11 and serving as the cathode and the electrode immersed in the plating bath and serving as the anode, to thereby deposit the metal ions contained in the plating bath on the surface of the metal-sputtered layer or alternatively metal-evaporated layer 6. In the electroplating method or the precision electroforming method, a solution of copper sulfate, cupric chloride, copper nitrate or the like is employed as the plating solution for plating with copper.

The IC element manufacturing method according to the instant exemplary embodiment is so arranged that the required conductive pattern inclusive of coils is first formed on the finished wafer 11, whereon the finished wafer 11 is scribed to thereby obtain the desired IC element 1. Thus, the IC elements each formed integrally with the coil can be manufactured

with high efficiency at lower manufacturing cost when compared with the case where the individual coils are each formed on the individual IC elements, respectively. Besides, it is possible to form the coils in a uniform thickness, respectively, for all the IC elements formed on the wafer with high precision, as a result of which dispersion or variance of the communication characteristics can be diminished. Furthermore, if the coil is formed for each of the individual IC elements by using the sputtering method or alternatively the vacuum evaporation method and the plating method, unwanted electrical conductor materials will be deposited on the outer peripheral portion of the IC element, giving rise to a problem in respect to the insulation quality of the IC element. Similarly, in the case the required conductive pattern inclusive of the coil is formed on the finished wafer 11, unwanted conductive materials may be deposited on the outer peripheral portion of the finished wafer 11 upon sputtering or the like process. However, since the outer peripheral portion mentioned above is intrinsically destined to be disposed of as the unwanted portion, adverse influence to the insulation quality of the individual IC elements can be avoided. Additionally, in the IC element manufacturing method according to the instant example, the metal-plated layer 7 is formed in the state where the photoresist layer 12 has been deposited, and thereafter the

portions of the metal-sputtered layer or alternatively metal-evaporated layer 6 where the metal-plated layer 7 is not laminated are removed by etching. Thus, the metal-plated layer 7 is laminated only on the top surface of the metal-sputtered layer or alternatively metal-evaporated layer 6 without spreading widthwise. Owing to these features, the antenna coil 3 can be formed with high accuracy or precision, which in turn means that the antenna coil 3 having an increased number of turns can be formed within a narrow space.

On the other hand, in the case of the IC element manufacturing method according to a second exemplary embodiment shown in Fig. 5, a photoresist layer 12 is uniformly formed over the surface passivation film 2 formed on the finished wafer 11 and then the photoresist layer 12 as formed is covered with a mask 13 of a required pattern inclusive of coils, whereon the photoresist layer 12 is exposed to illumination of light rays 14 of a predetermined wavelength externally of the mask 13, as is shown in Fig. 5A. Thereafter, the photoresist layer 12 exposed undergoes a developing process, whereby the light-exposed portions of the photoresist layer 12 are removed so that the portions of the surface passivation film 2 which correspond to the above-mentioned light exposure pattern are exposed externally as is shown in Fig. 5B. The light exposure pattern for the photoresist layer 12 can be so formed as to include an

electrode portion 15, antenna coils 3 and lead portions 16, as is shown in Fig. 6. Subsequently, the finished wafer 11 undergone the developing process is mounted on a sputtering apparatus or a vacuum evaporation apparatus and then the metal-sputtered layer or alternatively metal-evaporated layer 6 is formed on the exposed portions of the surface passivation film 2 mentioned above, as is shown in Fig. 5C. In succession, the photoresist layer 12 remaining deposited on the finished wafer 11 is removed through the ashing or like process, as is shown in Fig. 5D. Thereafter, by employing the above-mentioned electrode portion 15 as one electrode, electroplating is performed on the metal-sputtered layer or alternatively metal-evaporated layer 6, to thereby laminate the metal-plated layer 7 on the exposed portions of the metal-sputtered layer or alternatively metal-evaporated layer 6, as is shown in Fig. 5E. Finally, the finished wafer 11 mentioned above is scribed for thereby obtaining the desired IC element 1 shown in Fig. 1.

Incidentally, in the exemplary embodiments described above, the electroplating method is adopted as the means for forming the metal-plated layer 7. It should however be understood that instead of such method, an electroless plating method may be adopted for forming the metal-plated layer 7 mentioned above. In that case, since no electrode is required for forming the metal-plated layer 7, it is unnecessary to

form the electrode portion 15 and the lead portions 16 upon exposure of the photoresist layer 12 to the light rays.

The IC element manufacturing method according to the instant example can assure the similar advantageous effects as those of the IC element manufacturing method according to the first exemplary embodiment and additionally allows the number of the steps of forming the conductor pattern on the finished wafer 11 to be decreased, whereby the IC element formed integrally with the antenna coil can be manufactured at higher efficiency.

<Information carrier>

In the following, description will be made of information carriers according to exemplary embodiments of the present invention by reference to Figs. 7 to 17. Figure 7 is a plan view of an information carrier according to a first exemplary embodiment with a portion being broken away, Fig. 8 is a developed perspective view showing the information carrier according to the first exemplary embodiment, Fig. 9 is a sectional view of the information carrier according to the first exemplary embodiment, Fig. 10 is a view showing the information carrier according to the first exemplary embodiment in the state being used, Fig. 11 is a sectional view of an information carrier according to a second exemplary embodiment, Fig. 12 is a sectional view of an information carrier according to a

third exemplary embodiment, Fig. 13 is a sectional view of an information carrier according to a fourth exemplary embodiment, Fig. 14 is a sectional view of an information carrier according to a fifth exemplary embodiment, Fig. 15 is a sectional view of an information carrier according to a sixth exemplary embodiment, Fig. 16 is a sectional view of an information carrier according to a seventh exemplary embodiment, and Fig. 17 is a sectional view of an information carrier according to an eighth exemplary embodiment.

An information carrier 20a according to the first exemplary embodiment is comprised of a coin-like substrate 21 formed circularly in the planar shape and an IC element 1 mounted on the substrate 21 at a center portion as viewed planewise and thicknesswise of the substrate, as is shown in Figs. 7 to 9. As the IC element 1, the IC element which is formed integrally with the antenna coil, as shown in Fig. 1 and Fig. 2, is employed.

The substrate 21 is composed of a top member 22, an intermediate member 23 and a bottom member 24 which are integrally bonded together through interposed adhesive layers 25, respectively, as is shown in Fig. 8 and Fig. 9. Each of individual members 22, 23 and 24 constituting the substrate 21 may be formed of a paper sheet or a plastics sheet. However, it is preferred above all to form these members of paper sheets,

respectively, in consideration of their susceptibility to the spontaneous decomposition after having been scrapped, less generation of harmful gases in incineration and inexpensiveness. Of course, it is possible to form one or two of the members 22, 23 and 24 of a paper sheet with the other one or two members being formed of a plastics sheet.

Formed in the intermediate member 23 at a center portion thereof is a through-hole 27 into which the IC element 1 can be inserted. Thus, by bonding together the members 22, 23 and 24, a chamber in which the IC element 1 can be accommodated is formed. Incidentally, the IC element 1 should preferably be bonded fixedly to the bottom member 24 with a view to protecting the IC element from quaking upon handling of the information carrier. In that case, it is preferred from the standpoint of the manufacturing cost to form uniformly the adhesive layer 25 over one surface of the bottom member 24 so that bonding of the intermediate member 23 and the bottom member 24 on one hand and the bonding of the bottom member 24 and the IC element 1 on the other hand can be realized by making use of the adhesive layer 25. Further, the planar shape of the through-hole 27 may be selected arbitrarily. However, it is preferred from the manufacturing viewpoint to form the through-hole 27 in a circular shape, as shown in Fig. 7 and Fig. 8, because in that case there arises no necessity for precise alignment of orientation of

the IC element 1 in the rotational direction with a recess which is formed by bonding together the intermediate member 23 and the bottom member 24, when the IC element is placed in that recess.

By virtue of such arrangement that the IC element 1 is disposed at a center portion of the substrate 21 formed in a circular form as viewed in the planar direction, i.e., perpendicularly to the plane of the substrate, in the case of the information carrier 20a according to the instant exemplary embodiment, the information carrier 20 can be placed within a slot 101 formed substantially semicircularly in a reader/writer 100 equipped with an antenna coil 102 for contactless communication and disposed at a center of an arcuate portion of the slot 101. In that case, the antenna coil 3 formed integrally with the IC element 1 can automatically be centered or aligned with the antenna coil 102 of the reader/writer 100, as can be seen in Fig. 10, whereby the electromagnetic coupling between both the coils 3 and 102 can be increased, as a result of which electric power supply to the information carrier 20 from the reader/writer 100 as well as signal transmission/reception between the reader/writer 100 and the information carrier 20 can be carried out with high reliability. Furthermore, because the information carrier 20a is shaped in a circular form as viewed in the planar direction, i.e., perpendicularly to the plane of the information carrier, the information

carrier exhibits no directivity relative to the slot 101 formed substantially semicircularly, whereby excellent handleability of the information carrier can be ensured. Besides, because the IC element 1 is completely embedded within the substrate 21, not only high protection effectivity and excellent durability but also good aesthetic appearance owing to invisibility of the IC element 1 can be ensured for the information carrier.

Referring to Fig. 11, an information carrier 20b according to the second embodiment includes a substrate 21 constituted by a top member 22, an intermediate member 23 and a bottom member 24 and features disposition of a booster coil 28 in a concentric circular array around the IC element 1. In the figure, reference numeral 29 denotes a recess for accommodating therein the booster coil 28, wherein the recess is formed in a ring-like shape around a through-hole 27 of the intermediate member 23. In the other respects, the structure of the information carrier according to the second exemplary embodiment is identical with that of the information carrier 20a according to the first exemplary embodiment. Accordingly, repeated description thereof is omitted. The information carrier 20b according to the instant exemplary embodiment presents similar advantageous effects as those of the information carrier 20a according to the first exemplary embodiment. In

addition, by virtue of the concentric circular disposition of the booster coil 28 aground the IC element 1, the electromagnetic coupling between the antenna coil 3 formed integrally with the IC element 1 and the antenna coil 102 of the reader/writer 100 can be increased owing to interposition of the booster coil 28, whereby stabilization of the electric power as well as stabilization of the signal transmission/reception can further be enhanced with the communication range being also increased.

Referring to Fig. 12, an information carrier 20c according to the third exemplary embodiment includes a substrate 21 which is constituted by two members, i.e., a top member 22 and a bottom member 24, and features a recess 30 formed in the bottom member 24 for accommodating therein the IC element 1. In the other respects, the structure of the information carrier 20c according to the third exemplary embodiment is identical with that of the information carrier 20a according to the first exemplary embodiment. Accordingly, repeated description thereof is omitted. The information carrier 20c according to the instant exemplary embodiment presents similar advantageous effects as those of the information carrier 20a according to the first exemplary embodiment. Besides, because the number of the parts constituting the information carrier is small, more inexpensive implementation of the information carrier can be

realized.

Referring to Fig. 13, the information carrier 20d according to the fourth exemplary embodiment includes a substrate 21 which is constituted by two members, i.e., a top member 22 and a bottom member 24, and features a first recess 30 formed in the bottom member 24 for accommodating therein the IC element 1 and a second recess 29 formed for accommodating therein a booster coil 28. In the other respects, the structure of the information carrier 20d according to the third exemplary embodiment is identical with that of the information carrier 20c according to the third exemplary embodiment. Accordingly, repeated description thereof is omitted. The information carrier 20c according to the instant exemplary embodiment presents similar advantageous effects as those of the information carrier 20b according to the second exemplary embodiment. Besides, because the number of the parts constituting the information carrier is small, more inexpensive implementation of the information carrier can be realized.

Referring to Fig. 14, the information carrier 20e according to the fifth exemplary embodiment includes a substrate 21 which is constituted by two members, i.e., a top member 22 in which a through-hole 27 for accommodating therein the IC element and a bottom member 24 in which no through-hole 27 is formed, and features that the IC element 1 is accommodated

within a recess formed by bonding together the top member 22 and the bottom member 24 with the interior of the recess being sealed off by filling a potting resin 31. In the other respects, the structure of the information carrier 20e according to the fifth exemplary embodiment is identical with that of the information carrier 20a according to the first exemplary embodiment. Accordingly, repeated description thereof is omitted. The information carrier 20e according to the instant exemplary embodiment exhibits similar advantageous effects as those of the information carrier 20a according to the first exemplary embodiment except that the IC element 1 is not covered with the substrate.

Referring to Fig. 15, the information carrier 20f according to the sixth exemplary embodiment features a substrate 21 constituted by two members, i.e., a top member 22 in which a through-hole 27 for accommodating therein the IC element and a recess 29 for accommodating a booster coil are concentrically formed around a through-hole 27 and a bottom member 24 which has neither the through-hole 27 nor the recess 29, wherein the booster coil 28 is placed within the recess 29 with the recess 29 being sealed off with a potting resin 31 while the IC element 1 is accommodated within a recess formed by bonding together the top member 22 and the bottom member 24 with that recess also being sealed off with the potting resin 31. In

the other respects, the structure of the information carrier 20f according to the sixth exemplary embodiment is identical with that of the information carrier 20e according to the fifth exemplary embodiment. Accordingly, repeated description thereof is omitted. The information carrier 20f according to the instant exemplary embodiment exhibits similar advantageous effects as those of the information carrier 20a according to the first exemplary embodiment except that the IC element 1 is not covered with the substrate.

Referring to Fig. 16, the information carrier 20g according to the seventh exemplary embodiment features a substrate 21 constituted by a single member having one surface formed with a recess 30 for accommodating the IC element 1, which recess is sealed off with a potting resin 31 after the IC element 1 has been disposed therein. In the other respects, the structure of the information carrier 20g according to the seventh exemplary embodiment is identical with that of the information carrier 20e according to the fifth exemplary embodiment. Accordingly, repeated description thereof is omitted. The information carrier 20g according to the instant exemplary embodiment presents similar advantageous effects as those of the information carrier 20e according to the fifth exemplary embodiment. Besides, because the number of the parts constituting the information carrier is small, more inexpensive implementation of the

information carrier can be realized.

Referring to Fig. 17, the information carrier 20h according to the eighth exemplary embodiment features a substrate 21 constituted by a single member which has one surface formed with a first recess 30 for accommodating therein the IC element 1 and a second recess 29 for accommodating therein a booster coil 28, wherein the IC element 1 is disposed within the first recess 30 mentioned above with this recess being sealed off with a potting resin 31 while the booster coil 28 is accommodated within the second recess 29 mentioned above with this recess being also sealed off with the potting resin 31. In the other respects, the structure of the information carrier 20h according to the eighth exemplary embodiment is identical with that of the information carrier 20g according to the seventh exemplary embodiment. Accordingly, repeated description thereof is omitted. The information carrier 20h according to the instant exemplary embodiment presents similar advantageous effects as those of the information carrier 20f according to the sixth exemplary embodiment. Besides, because the number of the parts constituting the information carrier is small, more inexpensive implementation of the information carrier can be realized.

At this juncture, it is to be mentioned that in the exemplary embodiments described above, the substrate 21 is formed circularly as viewed in the

planar direction, i.e., perpendicularly to the plane of the substrate. It should however be appreciated that the substrate may be formed in other appropriate shapes such as square, rectangle, triangle or polygon, etc..

Further, in the case of the information carriers according to the second, fourth sixth and eighth exemplary embodiments, the discrete booster coil 28 is disposed in the through-hole and the recess formed in the substrate 21. It should however be understood that the booster coil 28 can directly be formed on the member constituting the substrate 21 by printing, plating, sputtering or the like process.

Furthermore, by implementing the booster coil 28 with a first coil for performing contactless communication with the IC element and a second coil of a greater capacity than the first coil for performing communication with an external reader/writer with and interconnecting the first and second coils in series to each other, the communication range or coverage can be extended.

<Method of manufacturing the information carrier>

Next, exemplary embodiments of the information carrier manufacturing method according to the present invention will be described by reference to Fig. 18 to Fig. 22. Figure 18 is a fragmental perspective view showing a first example of a strip material employed in manufacturing an information carrier according to the present invention, Fig. 19 is

a fragmental perspective view showing a second example of the strip material, Fig. 20 is a fragmental perspective view showing a third example of the strip material, Fig. 21 is a fragmental perspective view showing a fourth example of the strip material, and Fig. 22 is a fragmental perspective view showing a fifth example of the strip material.

In the information carrier manufacturing method according to the present invention, required parts to be mounted inclusive of the IC element 1 are disposed fixedly on a raw material (strip material) for implementing a unitary substrate formed in a strip-like shape, whereon other strip material or materials is bonded onto one or both surfaces of the strip material, as the case may be, or alternatively potting for the parts to be mounted are carried out, and thereafter the concerned information carriers are punched by die-cutting from the single or the unitary bonded strip. For carrying out the information carrier manufacturing method according to the present invention, there may be selectively employed a strip material 41 in which through-holes 27 for accommodating the IC elements 1, respectively, are formed with a constant interspace, as shown in Fig. 18, a strip material 42 in which through-holes 27 are formed with a constant interspace for accommodating the IC elements 1, respectively, and in which ring-shaped recesses 29 destined for accommodating booster coils 28, respectively, are

formed concentrically around the through-holes 27 with adhesive layers 32 being applied onto bottom surfaces of the ring-shaped recesses 29, respectively, as shown in Fig. 19, a strip material 43 in which recesses 30 are formed with a constant interspace for accommodating therein the IC elements 1, respectively, with an adhesive layer 32 being applied onto a bottom surface of each of the recesses 30, as shown in Fig. 20, a strip material 44 in which first recesses 30 are formed with a constant interspace for accommodating therein the IC elements 1, respectively, and in which second recesses 29 each of a ring-like shape are concentrically formed around the first recesses 30, respectively, with adhesive layers 32 being applied onto the bottom surfaces of the recesses 29 and 30, respectively, as shown in Fig. 21, or a strip material 45 on which neither through-holes nor recesses are formed but an adhesive layer 25 is uniformly applied over one surface of the strip material, as shown in Fig.22.

A first example of the information carrier manufacturing method according to the present invention is destined for manufacturing the information carrier 20a according to the first exemplary embodiment by using one sheet of strip material 41 shown in Fig. 18 and two sheets of strip materials 45 shown in Fig. 22. At first, one of the strip materials 45 is bonded to one surface of the strip material 41 with the adhesive layer 25 being interposed therebetween to thereby

obtain a unitary bonded strip composed of the strip materials 41 and 45 having spaces within which the IC elements 1 can be accommodated, respectively. Subsequently, the IC elements 1 are positioned to be placed within the spaces mentioned above, respectively, whereon the IC elements 1 are bonded to the strip material 45 by using the adhesive layers 25, respectively. In succession, the other strip material 45 is bonded to the other surface of the strip material 41 with the adhesive layer 25 interposed therebetween to thereby realize a unitary bonded strip composed of the strip materials 41 and 45 and having the IC elements 1 accommodated within the internal spaces, respectively. Finally, the unitary bonded strip is cut into segments each of a predetermined shape to obtain the information carriers 20a according to the first embodiment. With the information carrier manufacturing method according to the instant exemplary embodiment, a large number of the IC elements 1 are encased internally of the strip materials 41 and 45 and then the concerned information carriers are formed by punching from the bonded strip materials 41 and 45. Thus, the identical information carriers can be manufactured with high efficiency and hence the manufacturing cost of the information carrier can be reduced.

A second example of the information carrier manufacturing method according to the present invention is destined for manufacturing the information carrier

20b according to the second exemplary embodiment by using one sheet of the strip material 42 shown in Fig. 19 and two sheets of the strip materials 45 shown in Fig. 22. At first, the booster coils 28 are placed within ring-like recesses 29 formed in the strip material 42 and then the booster coil 28 are bonded to the bottom surfaces of the recesses 29 by using adhesive layers 32, respectively. Subsequently, the strip material 45 is bonded to one of the surfaces of the strip material 42 by using the adhesive layer 25 interposed therebetween to thereby obtain a unitary bonded strip composed of the strip materials 42 and 45 bonded together and having spaces within which the IC elements 1 can be accommodated, respectively. In succession, the IC elements 1 are positioned to be placed within the above-mentioned spaces and bonded to the strip material 45 with the adhesive layer 25. Thereafter, the other sheet of strip material 45 is bonded to the other surface of the strip material 41 with the adhesive layer 25 interposed therebetween to thereby obtain the bonded strip constituted by the strip materials 42 and 45 and having the IC elements 1 accommodated within the internal spaces, respectively. Next, the space within which the IC element 1 has been accommodated is filled with a potting resin 31 to obtain the unitary bonded strip composed of the strip materials 41 and 45 and having the IC elements 1 fixedly embedded therein. Finally, the unitary bonded

strip is cut into segments each of a predetermined shape to obtain the information carriers 20e according to the fifth exemplary embodiment. The instant example of the information carrier manufacturing method presents similar advantageous effects as those of the information carrier manufacturing method according to the first embodiment.

A third example of the information carrier manufacturing method according to the present invention is destined for manufacturing the information carrier 20c according to the third exemplary embodiment by using a single sheet of the strip material 43 shown in Fig. 20 and a single sheet of the strip material 45 shown in Fig. 22. At first, the IC elements 1 are positioned to be placed within the recesses 30, respectively, which are formed in the strip material 43 and then the IC elements are bonded to the bottom surfaces of the recesses 30 by using the adhesive layers 32, respectively. Subsequently, the strip material 45 is bonded to the surface of the strip material 43 formed with the recesses by using the adhesive layer 25 interposed therebetween to thereby obtain a unitary bonded strip which is composed of the strip materials 43 and 45 bonded together and having the IC elements 1 embedded therein. Finally, the unitary bonded strip is cut into segments each of a predetermined shape to thereby obtain the information carriers 20c according to the third exemplary

embodiment. The instant example of the information carrier manufacturing method presents similar advantageous effects as those of the information carrier manufacturing method according to the first embodiment.

A fourth example of the information carrier manufacturing method according to the present invention is destined for manufacturing the information carrier 20d according to the fourth exemplary embodiment by using a single sheet of the strip material 44 shown in Fig. 21 and a single sheet of the strip material 45 shown in Fig. 22. At first, the IC elements 1 are positioned to be placed within the first recesses 30, respectively, which are formed in the strip material 44, and then the IC elements are bonded to the bottom surfaces of the above-mentioned recesses 30 by using the adhesive layers 32, respectively, while the booster coils 28 are accommodated within the second ring-like recesses 29, respectively, which are formed in the strip material 44 and bonded to the bottom surfaces of the above-mentioned recesses 29, respectively, by using the adhesive layers 32 interposed therebetween. Subsequently, the strip material 45 is bonded to the surface of the strip material 44 having the recesses by using the adhesive layer 25 interposed therebetween to thereby obtain a unitary bonded strip which is composed of the strip materials 44 and 45 bonded together and having internal spaces within which the IC elements 1

have been accommodated, respectively. Finally, the unitary bonded strip is cut into segments each of a predetermined shape to obtain the information carriers 20c according to the third exemplary embodiment. The instant example of the information carrier manufacturing method presents similar advantageous effects as those of the information carrier manufacturing method according to the first embodiment.

A fifth example of the information carrier manufacturing method according to the present invention is destined for manufacturing the information carrier 20e according to the fifth exemplary embodiment by using a single strip material 41 shown in Fig. 18 and a single sheet of strip material 45 shown in Fig. 22. At first, the strip material 45 is bonded to one surface of the strip material 41 with the adhesive layer 25 being interposed therebetween to thereby obtain a bonded strip composed of the strip materials 41 and 45 and having the spaces within which the IC elements 1 can be accommodated, respectively. Subsequently, the IC elements 1 are positioned to be placed within the above-mentioned spaces, respectively, whereon the IC elements are bonded to the strip material 45 by using the adhesive layer 25 interposed therebetween. In succession, the spaces in which the above-mentioned IC elements 1 are accommodated, respectively, are each filled with the potting resin 31 to thereby obtain the unitary bonded strip constituted by the strip materials

41 and 45 and having the IC elements 1 embedded therein. Finally, the unitary bonded strip is cut into segments each of a predetermined shape to obtain the information carriers 20e according to the fifth exemplary embodiment. The instant example of the information carrier manufacturing method equally presents similar advantageous effects as those of the information carrier manufacturing method according to the first embodiment.

A sixth example of the information carrier manufacturing method according to the present invention is destined for manufacturing the information carrier 20f according to the sixth exemplary embodiment by using one sheet of the strip material 42 shown in Fig. 19 and a single sheet of the strip material 45 shown in Fig. 22. At first, the booster coils 28 are placed within the ring-like recesses 29, respectively, which are formed in the strip material 42, and then the booster coils 28 are bonded to the bottom surfaces of the recesses 29 by using the adhesive layers 32, respectively. Subsequently, the strip material 45 is bonded to one of the surfaces of the strip material 42 by using the adhesive layer 25 interposed therebetween to thereby obtain a bonded strip composed of the strip materials 42 and 45 bonded together and having the spaces within which the IC elements 1 can be accommodated, respectively. In succession, the IC elements 1 are positioned to be placed within the

above-mentioned spaces, respectively, and bonded to the strip material 45 with the adhesive layer 25 interposed therebetween. In succession, the recesses 29 in which the above-mentioned booster coils 28 are accommodated and the spaces in which the above-mentioned IC elements 1 are accommodated are each filled with the potting resin 31 to thereby obtain the unitary bonded strip constituted by the strip materials 42 and 45 and having the IC elements 1 and the booster coils 28 which are embedded therein. Finally, the unitary bonded strip is cut into segments each of a predetermined shape to obtain the information carriers 20f according to the sixth exemplary embodiment. The instant example of the information carrier manufacturing method equally presents similar advantageous effects as those of the information carrier manufacturing method according to the first embodiment.

A seventh example of the information carrier manufacturing method according to the present invention is destined for manufacturing the information carrier 20g according to the seventh exemplary embodiment by using a single sheet of the strip material 43 shown in Fig. 20. At first, the IC elements 1 are positioned to be accommodated within recesses 30, respectively, which are formed in the strip material 43 and then the IC elements are bonded to the bottom surfaces of the recesses 30, respectively, by using the adhesive layers 32, respectively. In succession, the recesses 30 in

which the above-mentioned IC elements 1 are accommodated are each filled with the potting resin 31 to thereby obtain the strip material 43 having the IC elements 1 embedded therein. Finally, this strip material 43 is cut into segments each of a predetermined shape to obtain the information carriers 20g according to the seventh exemplary embodiment. The instant example of the information carrier manufacturing method equally presents similar advantageous effects as those of the information carrier manufacturing method according to the first embodiment.

An eighth example of the information carrier manufacturing method according to the present invention is destined for manufacturing the information carrier 20h according to the eighth exemplary embodiment by using a single sheet of the strip material 44 shown in Fig. 21. At first, the IC elements 1 are positioned to be accommodated within the first recesses 30, respectively, which are formed in the strip material 43 and then the IC elements are bonded to the bottom surfaces of the recesses 30, respectively, by using the adhesive layers 32, respectively, while the booster coils 28 are accommodated within the second ring-like recesses 29, respectively, which are formed in the strip material 44 and then the booster coils are bonded to the bottom surfaces of the recesses 29 by using the adhesive layers 32, respectively. In succession, the first recesses 30 in which the above-mentioned IC

elements 1 are accommodated and the second recesses 29 in which the above-mentioned booster coils 28 are accommodated are each filled with the potting resin 31 to thereby obtain the strip material 43 having the IC elements 1 and the booster coils 28 embedded therein. Finally, this strip is cut into segments each of a predetermined shape to obtain the information carriers 20h according to the eighth exemplary embodiment. The instant example of the information carrier manufacturing method equally presents similar advantageous effects as those of the information carrier manufacturing method according to the first embodiment.

Incidentally, in the second, fourth, sixth and eighth exemplary embodiments described above, the booster coil 28 is formed separately or independently from the substrate 21, the booster coil 28 may be formed by printing on any one of the strip materials constituting the substrate 21.

INDUSTRIAL APPLICABILITY

As is apparent from the foregoing description, in the IC element according to the present invention, the electric conductor of the coil formed integrally with the IC element is implemented in a multilayer structure including the metal-sputtered layer or alternatively metal-evaporated layer and the metal-plated layer. Thus, when compared with the IC element in which the electric conductor is formed only

of the metal-sputtered layer or alternatively metal-evaporated layer, loss of the electromagnetic energy can be reduced, which can contribute to stabilization of electric power reception from the reader/writer, stabilization of communication with the reader/writer and extension of the communication range relative to the reader/writer.

In the IC element manufacturing method according to the present invention, a large number of coils corresponding to the individual IC elements, respectively, can simultaneously be formed in the finished wafer instead of forming the coil in each of the IC elements. Thus, the IC element formed internally with the coil can be manufactured with high efficiency, as a result of which this sort of IC element can be manufactured at low cost.

In the information carrier according to the present invention, the IC element formed integrally with the coil is disposed at a center portion of the substrate as viewed in the planar direction, i.e., perpendicularly to the plane of the substrate. Thus, the center of the coil formed integrally with the IC element and that of the antenna coil of the reader/writer can easily be aligned with each other, which means that the electromagnetic coupling coefficient between both the coils is increased, whereby the electric power supply to the information carrier from the reader/writer as well as the signal

transmission/reception between the reader/writer and the information carrier can be stabilized.

In the information carrier manufacturing method according to the present invention, the unitary strip in which the required parts to be mounted inclusive of the IC elements are mounted on the strip material is manufactured, whereon the concerned information carriers are formed by punching the unitary strip. Thus, the identical information carriers can be manufactured with high efficiency, whereby the cost involved in manufacturing the information carriers each incorporating the IC element can be reduced.

CLAIMS

1. An IC element formed integrally with a coil for performing contactless data communication with external equipment, characterized in that a conductor constituting said coil is implemented in a multilayer structure including a metal-sputtered layer or alternatively a metal-evaporated layer and a metal-plated layer.

2. An IC element set forth in claim 1, characterized in that said metal-sputtered layer or alternatively said metal-evaporated layer is formed of at least one metal of aluminum, nickel, copper and chromium or alternatively an alloy containing those metals and that said metal-plated layer deposited on said metal-sputtered layer or alternatively said metal-evaporated layer is formed of copper.

3. An IC element set forth in claim 1, characterized in that said coil is formed on a surface of said IC element formed with input/output terminals with interposition of an electrically insulative surface passivation film and that the input/output terminals of said IC element and said coil are electrically interconnected through through-holes formed in said surface passivation film and each having a diameter smaller than a line width of said coil.

4. An IC element set forth in claim 1, characterized in that said coil is implemented in a rectangular spiral pattern in a planar shape and that

all or some of corner portions of said rectangular spiral pattern are chamfered.

5. An IC element set forth in claim 1, characterized in that said metal-plated layer is formed by resorting to a electroless plating method or alternatively an electroplating method or alternatively a precision electroforming method.

6. An IC element set forth in claim 1, characterized in that a line width of said coil is not smaller than 7 μm, an inter-line distance thereof is not greater than 5 μm and the number of turns thereof is not smaller than 20 turns.

7. A method of manufacturing an IC element, characterized in that said method comprises a step of forming uniformly a metal-sputtered layer or alternatively a metal-evaporated layer on a surface passivation film of a finished wafer manufactured through a predetermined process, a step of forming uniformly a photoresist layer on said metal-sputtered layer or alternatively on said metal-evaporated layer, a step of forming in said photoresist layer a predetermined pattern inclusive of a coil for contactless data communication with external equipment through light exposure and development to thereby expose said metal-sputtered layer or alternatively said metal-evaporated layer through said predetermined pattern, a step of laminating a metal-plated layer on exposed portions of said metal-sputtered layer or

alternatively said metal-evaporated layer through an electroless plating method or alternatively an electroplating method or alternatively a precision electroforming method, a step of eliminating the photoresist layer deposited on said finished wafer, a step of forming a predetermined conductor pattern corresponding to said predetermined pattern by etching said metal-sputtered layer or alternatively said metal-evaporated layer exposed through said metal-plated layer, and a step of obtaining concerned IC elements each formed integrally with a coil by scribing said finished wafer.

8. A method of manufacturing an IC element, characterized in that said method comprises a step of forming uniformly a photoresist layer on a surface passivation film of a finished wafer manufactured through a predetermined process, a step of forming in said photoresist layer a predetermined pattern inclusive of a coil for contactless data communication with external equipment through light exposure and development to thereby expose said surface passivation film in said predetermined pattern, a step of mounting the finished wafer undergone a development processing on a sputtering apparatus or alternatively a vacuum evaporation apparatus and forming a metal-sputtered layer or alternatively a metal-evaporated layer on exposed portions of said surface protection film, a step of eliminating the photoresist layer deposited on

said finished wafer, a step of forming a metal-plated layer on said metal-sputtered layer or alternatively on said metal-evaporated layer by resorting to an electroless plating method or alternatively an electroplating method, and a step of obtaining concerned IC elements each formed integrally with a coil by scribing said finished wafer.

9. An information carrier including a substrate having mounted thereon an IC element formed integrally with an antenna coil for performing data communication in a contactless manner with external equipment, characterized in that said IC element is disposed at a center portion of said substrate in a planar direction perpendicularly to a plane of said substrate.

10. An information carrier set forth in claim 9, characterized in that both of top and bottom surfaces of said IC element are covered with said substrate.

11. An information carrier set forth in claim 9, characterized in that only one surface of said IC element is covered with said substrate.

12. An information carrier set forth in claim 9, characterized in that said substrate is formed in a circular or square planar shape.

13. An information carrier set forth in claim 9, characterized in that said substrate is wholly or partially formed of paper.

14. An information carrier set forth in claim 9, characterized in that said substrate is implemented in

a three-bonded-layer structure including a top member, a bottom member and an intermediate member and that said IC element is accommodated within a through-hole formed in said intermediate member at a mid portion thereof.

15. An information carrier set forth in claim 14, characterized in that said though-hole is formed circularly in a planar shape.

16. An information carrier set forth in claim 9, characterized in that said substrate is implemented in a two-bonded-layer structure including a top member and a bottom member and that said IC element is accommodated within a recess formed in said top member or alternatively in said bottom member at a mid portion thereof.

17. An information carrier set forth in claim 9, characterized in that said substrate is implemented in a single layer structure and that said IC element is accommodated within a recess formed in said substrate at a mid portion thereof.

18. An information carrier set forth in claim 16 or claim 17, characterized in that said recess is formed circularly in a plane shape.

19. An information carrier set forth in claim 9, characterized in that further comprising another discrete coil which is separately formed independent of said IC element internally of said substrate.

20. An information carrier manufacturing method,

characterized in that the method comprises a step of bonding together a first strip material having regularly formed therein a number of through-holes in which IC elements can be inserted, respectively, and a second strip material formed with no through-hole, a step of placing and fixing the IC elements each formed integrally with a coil in said through-holes, respectively, a step of bonding together said first strip material and a third strip material provided with no through-hole, and a step of punching said first to third strip materials bonded unitarily to thereby obtain the concerned information carriers each incorporating said IC element.

21. An information carrier manufacturing method, characterized in that the method comprises a step of placing and fixing coils formed separately independent of IC elements in a number of ring-like recesses formed in a first strip material concentrically around through-holes, respectively, which are formed regularly in said first strip material and capable of accommodating said IC elements, respectively, a step of bonding a second strip material having no through-hole onto one surface of said first strip material, a step of placing fixedly said IC elements each formed integrally with a coil in said through-holes, respectively, a step of bonding together said first strip material and a third strip material having no through-hole, and a step of punching said first to

third strip materials bonded unitarily to thereby obtain desired information carriers each including the IC element and the coil formed separately independent of said IC element.

22. An information carrier manufacturing method, characterized in that the method comprises a step of placing fixedly IC elements each formed integrally with a coil in a number of recesses for accommodating the IC elements, respectively, which recesses are regularly formed in a first strip material, a step of bonding a second strip material having no through-hole onto a surface of said first strip material in which no through-holes are formed, and a step of punching the first and second strip materials bonded unitarily to thereby obtain desired information carriers each incorporating said IC element.

23. An information carrier manufacturing method, characterized in that the method comprises a step of placing fixedly IC elements each formed integrally with a coil in a number of first recesses formed regularly in a first strip material which has second recesses each formed in a ring-like shape concentrically around said first recesses, respectively, said first recesses being capable of accommodating said IC elements, respectively, a step of placing fixedly coils formed discretely independent of said IC elements within said second recesses, respectively, formed in said first strip material, a step of bonding a second strip

material having no through-hole onto a surface of said first strip material in which said recesses are formed, and a step of punching said first and second strip materials bonded unitarily to thereby obtain desired information carriers each including the IC element and the coil formed discretely independent of said IC element.

24. An information carrier manufacturing method, characterized in that the method comprises a step of bonding together a first strip material having a number of through-holes formed regularly and allowing IC elements to be inserted therein, respectively, and a second strip material having no through-hole, a step of placing and fixing said IC elements each formed integrally with a coil in said through-holes, respectively, a step of sealing off said through-holes having said IC elements accommodated therein, and a step of punching the first and second strip materials bonded unitarily to thereby obtain desired information carriers each incorporating said IC element.

25. An information carrier manufacturing method, characterized in that the method comprises a step of placing and fixing coils formed separately independent of IC elements in a number of ring-like recesses formed in a first strip material concentrically around through-holes, respectively, which are formed regularly in said first strip material and capable of accommodating said IC elements, respectively, a step of

bonding together said first strip material and a second strip material having no through-hole, a step of sealing off said through-holes having said coils accommodated therein with a resin, and a step of punching said first and second strip materials bonded unitarily to thereby obtain desired information carriers each including said IC element and the associated coil formed separately independent of said IC element.

26. An information carrier manufacturing method, characterized in that the method comprises a step of placing fixedly IC elements each formed integrally with a coil in a number of recesses for accommodating said IC elements, respectively, said recesses being regularly formed in a strip material, a step of sealing off said recesses having said IC elements accommodated therein with a resin, and a step of punching said strip material to thereby obtain desired information carriers each incorporating said IC element.

27. An information carrier manufacturing method, characterized in that the method comprises a step of placing fixedly IC elements each formed integrally with a coil in a number of first recesses, respectively, which are formed regularly in a strip material having second ring-like recesses formed concentrically around said first recesses, respectively, said first recesses being capable of accommodating said IC elements, respectively, a step of placing fixedly coils formed

discretely independent of said IC elements within said second recesses, respectively, of said strip material, a step of sealing off said first and second recesses with a resin, and a step of punching said strip material to thereby obtain desired information carriers each including the IC element and the coil formed discretely independent of said IC element.

FIG. 1A

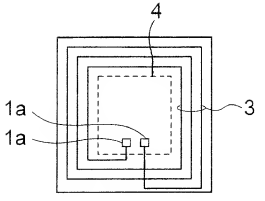


FIG. 1B

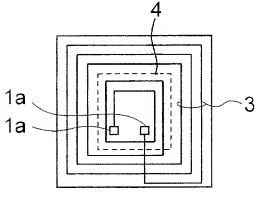


FIG. 1C

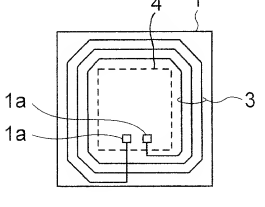


FIG. 2A

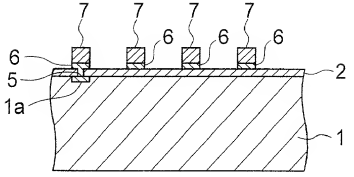


FIG. 2B

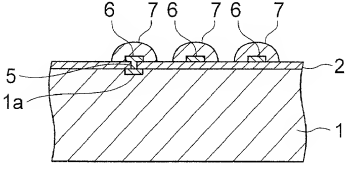


FIG. 3

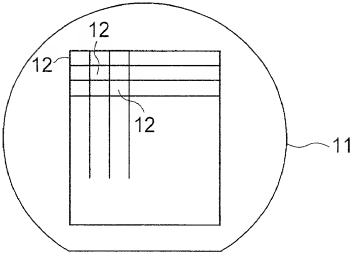


FIG. 4A

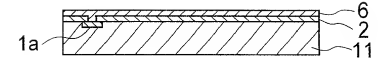


FIG. 4B

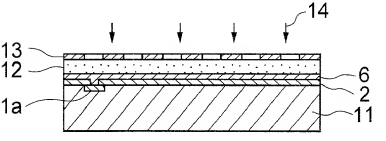


FIG. 4C

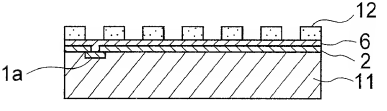


FIG. 4D

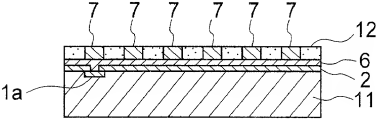


FIG. 4E

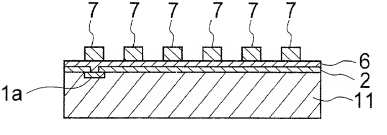


FIG. 4F

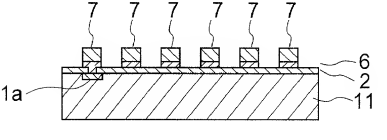


FIG. 5A

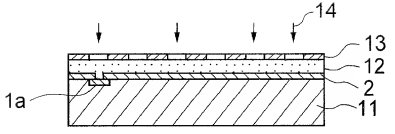


FIG. 5B

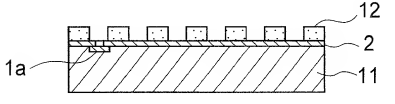


FIG. 5C

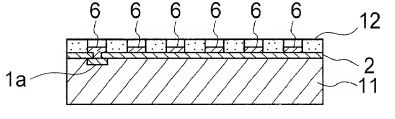


FIG. 5D

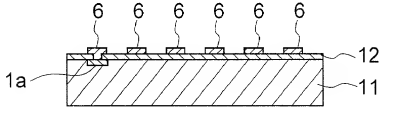


FIG. 5E

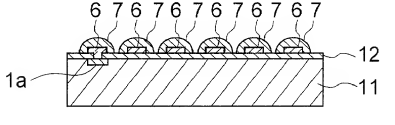


FIG. 6

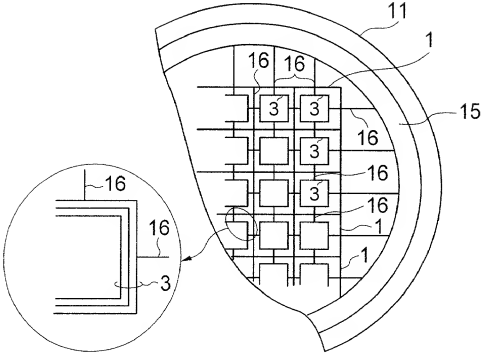


FIG. 7

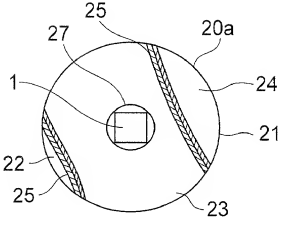


FIG. 8

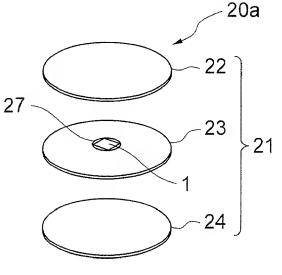


FIG. 9

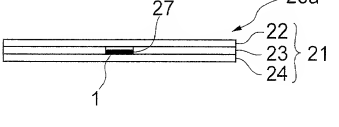


FIG. 10

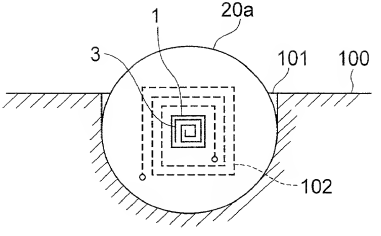


FIG. 11

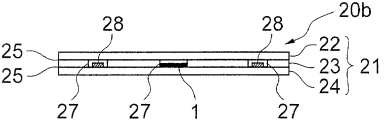


FIG. 12

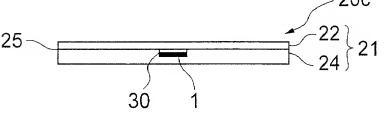


FIG. 13

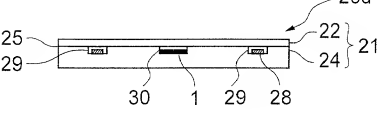


FIG. 14

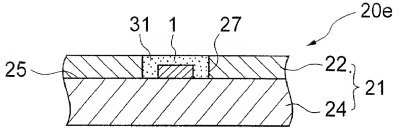


FIG. 15

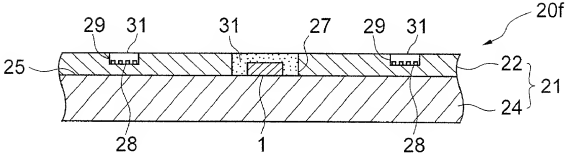


FIG. 16

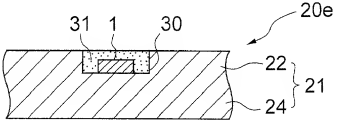


FIG. 17

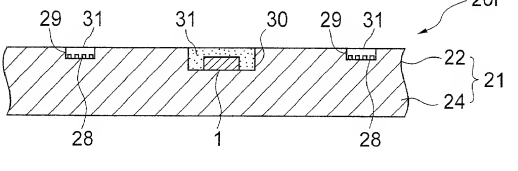


FIG. 18

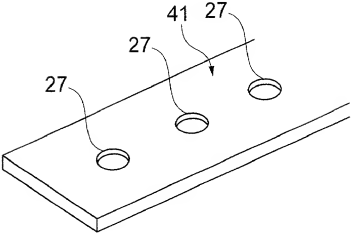


FIG. 19

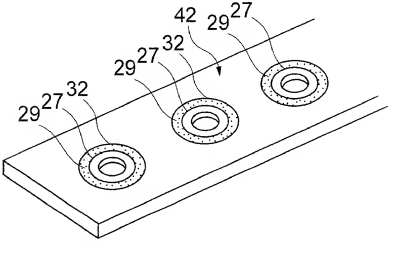


FIG. 20

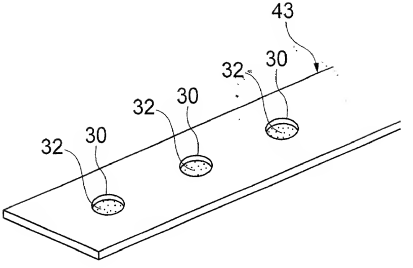


FIG. 21

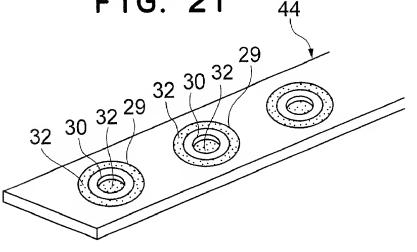
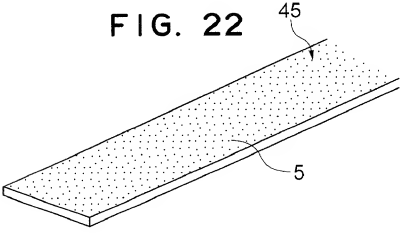


FIG. 22



BIRCH, STEWART, KOLASCH & BIRCH, LLP

PLEASE NOTE: YOU MUST COMPLETE THE FOLLOWING:

COMBINED DECLARATION AND POWER OF ATTORNEY FOR PATENT AND DESIGN APPLICATIONS

ATTORNEY DOCKET NO. 0152-0577P

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated next to my name; that I verily believe that I am the original, first and sole inventor (if only one inventor is named below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Insert Title: "IC DEVICE AND ITS PRODUCTION METHOD, AND INFORMATION CARRIER MOUNTED WITH IC DEVICE AND ITS PRODUCTION METHOD"

Fill in Appropriate Information - For Use Without Specification Attached:

the specification of which is attached hereto. If not attached hereto,

the specification was filed on _____ as

United States Application Number _____; and /or

the specification was filed on February 23, 2000 as PCT

International Application Number PCT/JP00/01029; and was

amended under PCT Article 19 on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.

I do not know and do not believe the same was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (six months for designs) prior to this application, and that no application for patent or inventor's certificate on this invention has been filed in any country foreign to the United States of America prior to this application by me or my legal representatives or assigns, except as follows.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 (a)-(d) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Insert Priority Information: (if appropriate)

Prior Foreign Application(s)			Priority Claimed	
11-046545 (Number)	Japan (Country)	Feb. 24, 1999 (Month/Day/Year Filed)	☒ Yes	☐ No
11-059753 (Number)	Japan (Country)	March 8, 1999 (Month/Day/Year Filed)	☒ Yes	☐ No
(Number)	(Country)	(Month/Day/Year Filed)	☐ Yes	☐ No
(Number)	(Country)	(Month/Day/Year Filed)	☐ Yes	☐ No
(Number)	(Country)	(Month/Day/Year Filed)	☐ Yes	☐ No

Insert Provisional Application(s): (if any)

I hereby claim the benefit under Title 35, United States Code, §119(e) of any United States provisional application(s) listed below.

(Application Number) (Filing Date)

(Application Number) (Filing Date)

Insert Requested Information: (if appropriate)

All Foreign Applications, if any, for any Patent or Inventor's Certificate Filed More Than 12 Months (6 Months for Designs) Prior To The Filing Date of This Application:

Country	Application No.	Date of Filing (Month/Day/Year)

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

Insert Prior U.S. Application(s): (if any)

(Application Number)	(Filing Date)	(Status - patented, pending, abandoned)

I hereby appoint the following attorneys to prosecute this application and/or an international application based on this application and to transact all business in the Patent and Trademark Office connected therewith and in connection with the resulting patent based on instructions received from the entity who first sent the application papers to the attorneys identified below, unless the inventor(s) or assignee provides said attorneys with a written notice to the contrary:

Terrell C. Birch	(Reg. No. 19,382)	Raymond C. Stewart	(Reg. No. 21,066)
Joseph A. Kolasch	(Reg. No. 22,463)	James M. Slattery	(Reg. No. 28,380)
Bernard L. Sweeney	(Reg. No. 24,448)	Michael K. Mutter	(Reg. No. 29,680)
Charles Gorenstein	(Reg. No. 29,271)	Gerald M. Murphy, Jr.	(Reg. No. 28,977)
Leonard R. Svensson	(Reg. No. 30,330)	Terry L. Clark	(Reg. No. 32,644)
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PLEASE NOTE: YOU MUST COMPLETE THE FOLLOWING:

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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